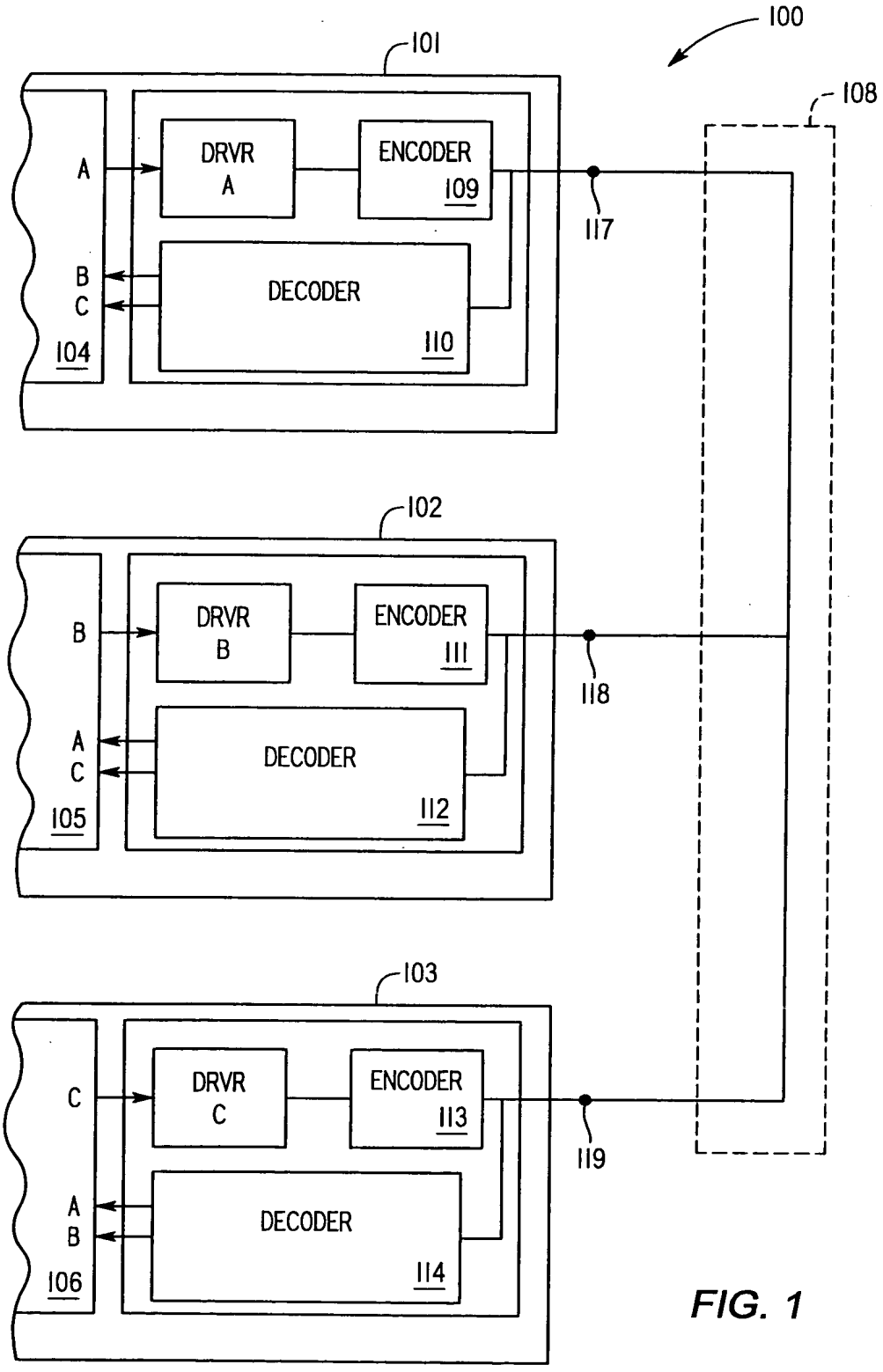

100
101
108
A
DRVR
A
ENCODER
109
117
B
C
DECODER
110
104
102
B
DRVR
B
ENCODER
111
118
A
C
DECODER
112
105
103
C
DRVR
C
ENCODER
113
119
A
B
DECODER
114
106

FIG. 1

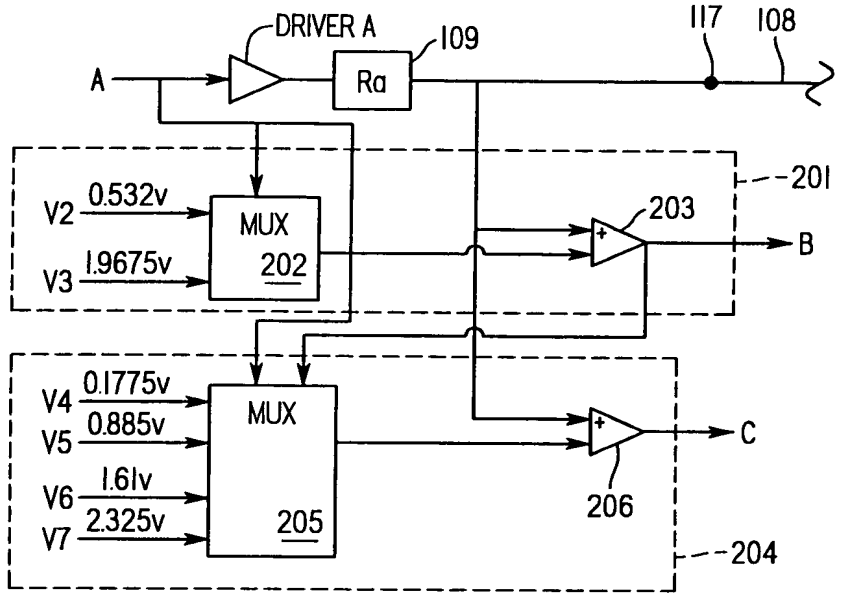

DRIVER A
109
117
108
A
Ra
201
V2
0.532v
MUX
202
203
B
V3
1.9675v
V4
0.1775v
V5
0.885v
MUX
C
V6
1.61v
V7
2.325v
205
206
204

FIG. 2

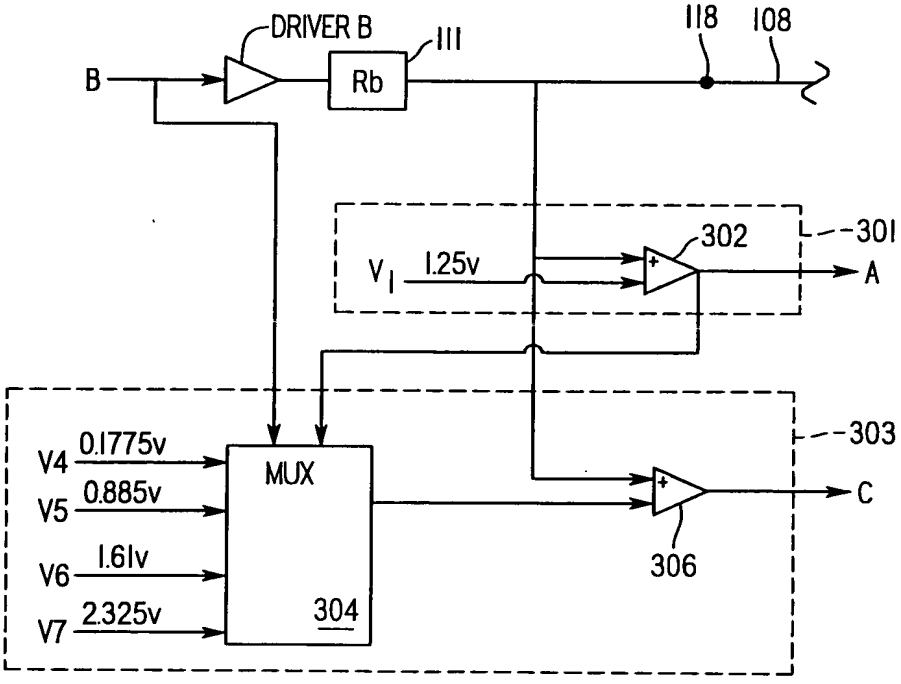

DRIVER B
111
118
108
B
Rb
302
301
V1
1.25v
A
V4
0.1775v
V5
0.885v
MUX
303
C
V6
1.61v
V7
2.325v
304
306

FIG. 3

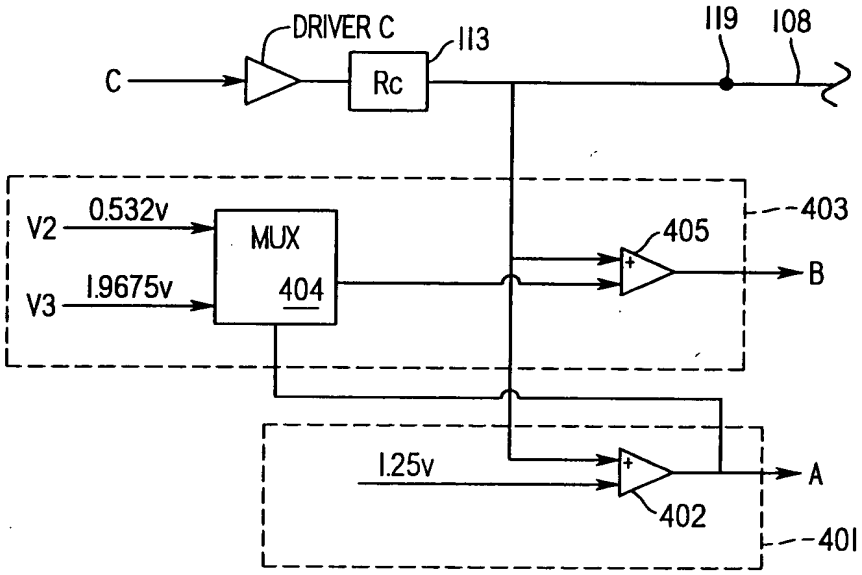

DRIVER C
113
C
Rc
119
108
403
V2
0.532v
MUX
405
B
V3
1.9675v
404
1.25v
A
402
401

FIG. 4

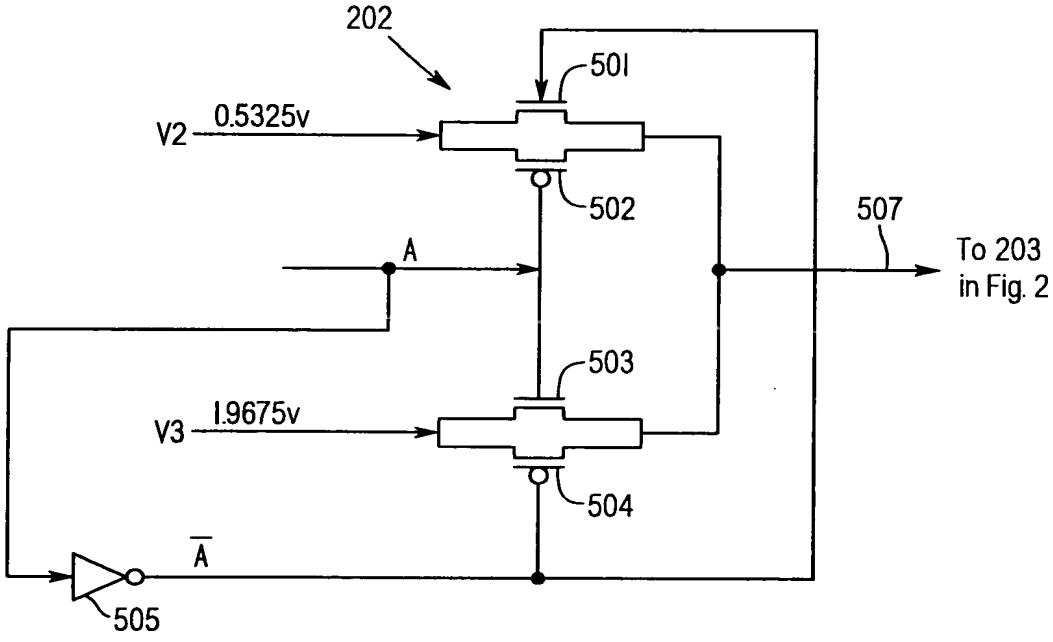
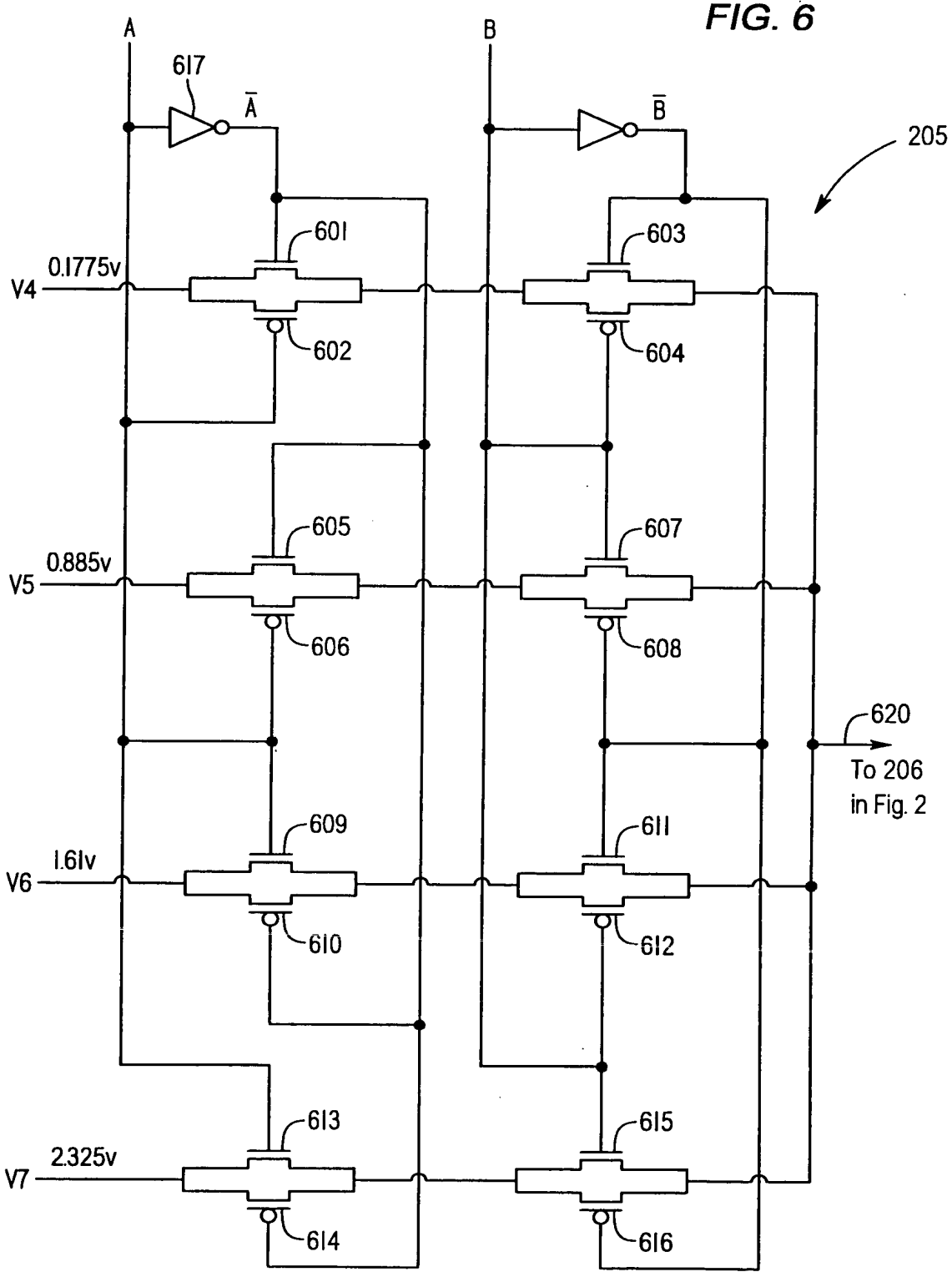

202
501
V2
0.5325v
502
507
To 203
in Fig. 2
A
503
V3
1.9675v
504
$\overline{A}$
505

FIG. 5

FIG. 6


A
B
617
$\bar{A}$
$\bar{B}$
205
601
603
0.1775v
V4
602
604
605
607
0.885v
V5
606
608
620
To 206
in Fig. 2
609
611
1.61v
V6
610
612
613
615
2.325v
V7
614
616

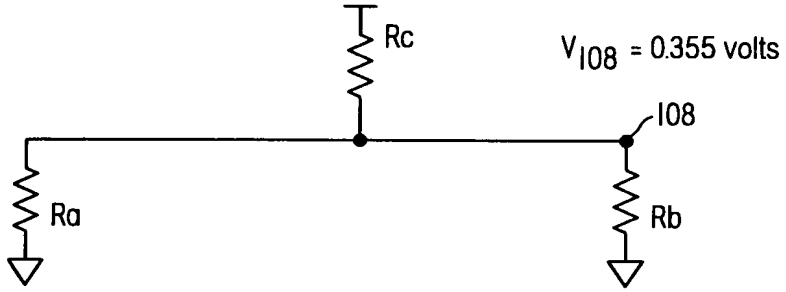


FIG. 7

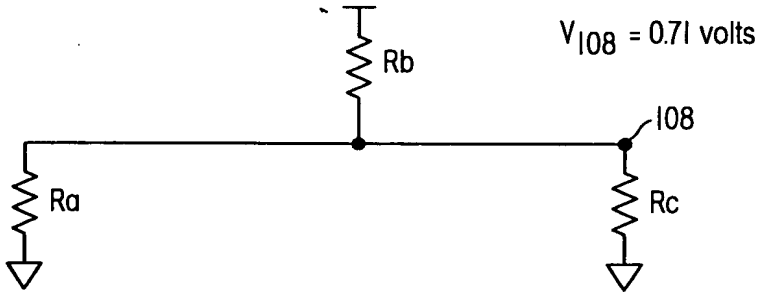


FIG. 8

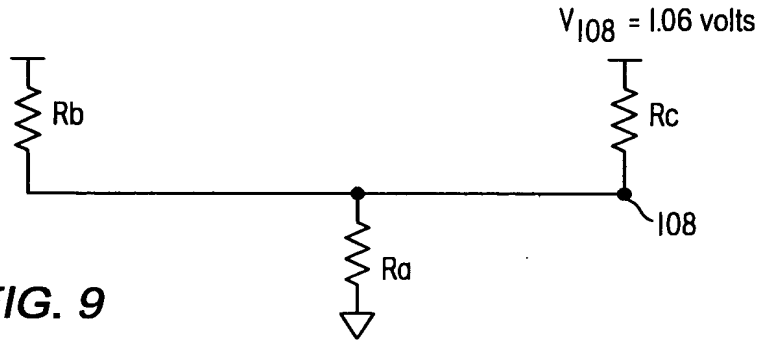


FIG. 9